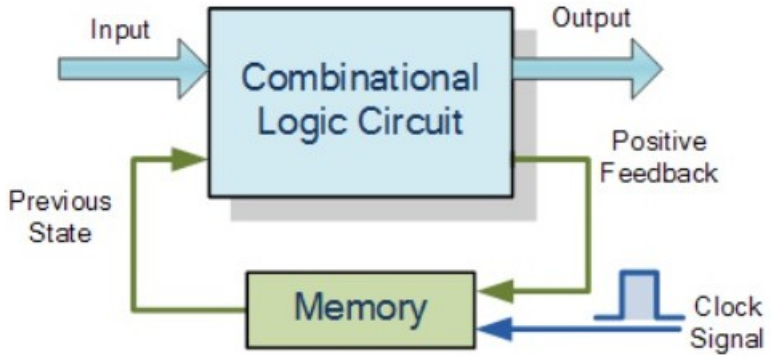
Sequential Logic Circuits

We studied the logic circuits whose outputs at any instant of time depend only on the input signals present at that time are known as combinational circuits. Moreover, in a combinational circuit, the output appears immediately for a change in input, except for the propagation delay through circuit gates.

In sequential logic the output of the logic device is dependent not only on the present inputs to the device, but also on past inputs; i.e., the output of a sequential logic device depends on its present internal state and the present inputs. This implies that a sequential logic device has some kind of memory of at least part of its "history" (i.e., its previous inputs).

In sequential circuits, the output signals are fed back to the input side. A block diagram of a sequential circuit is shown in Figure below:-



Latches and flip-flops are commonly used memory devices in sequential circuits. Basically, latches and flip-flops are memory devices which can assume one of two stable output states and which have one or more inputs that can cause the output state to change.

FLIP – FLOPS

The basic 1-bit digital memory circuit is known as a flip-flop. It can have only two states, either the 1 state or the 0 state. A flip-flop is also known as a bistable multivibrator. Flip-flops can be obtained by using NAND or NOR gates.

TYPES OF FLIP-FLOPS

There are different types of flip-flops depending on how their inputs and clock pulses cause transition between two states. We will discuss different types of flip-flops such as: S-R, D, J-K, T and Master-Slave. Basically D, J-K, and T are three different modifications of the S-R flip-flop.

The Set-Reset (S-R) Flip-Flop.

An S-R flip-flop has two inputs named Set (S) and Reset (R), and two outputs Q and Q'. The outputs are complement of each other, i.e., if one of the outputs is 0 then the other should be 1. This can be implemented using NAND or NOR gates. The NAND gate S-R flip-flop is shown in Figure below:-

The Set State

Consider the circuit shown above. If the input R is at logic level "0" (R = 0) and input S is at logic level "1" (S = 1), the NAND gate **Y** has at least one of its inputs at logic "0" therefore, its output Q' must be at a logic level "1" (NAND Gate principles). Output Q' is also fed back to input "A" and so both inputs to NAND gate **X** are at logic level **'1'**, and therefore its output Q must be at logic level "0".

Reset State

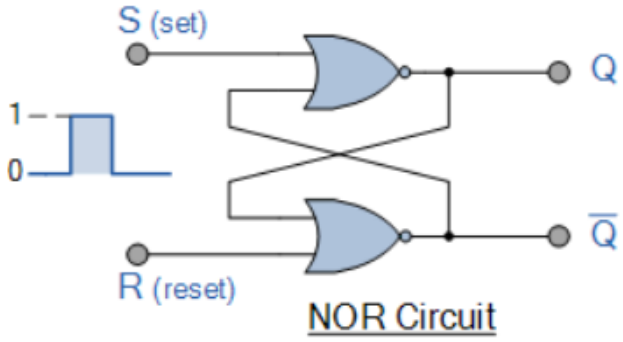
In this second stable state, Q' is at logic level "0", (not Q = "0") its inverse output at Q is at logic level "1", (Q = "1"), and is given by R = "1" and S = "0". As gate *X* has one of its inputs at logic "0" its output Q must equal logic level "1" (again NAND gate principles). Output Q is fed back to input "B", so both inputs to NAND gate *Y* are at logic "1", therefore, Q' = "0".

Truth Table for this Set-Reset Function

State	S	R	Q		Description
Set	1	0	0	1	Set $\overline{Q}$ » 1
	1	1	0	1	no change
Reset	0	1	1	0	Reset $\overline{Q}$ » 0
	1	1	1	0	no change
Invalid	0	0	1	1	Invalid Condition

The NOR Gate S-R Flip-flop

An S-R flip-flop can be constructed with NOR gates at ease by connecting the NOR gates back to back as shown in Figure below. The cross-coupled connections from the output of gate 1 to the input of gate 2 constitute a feedback path.



NOR Circuit

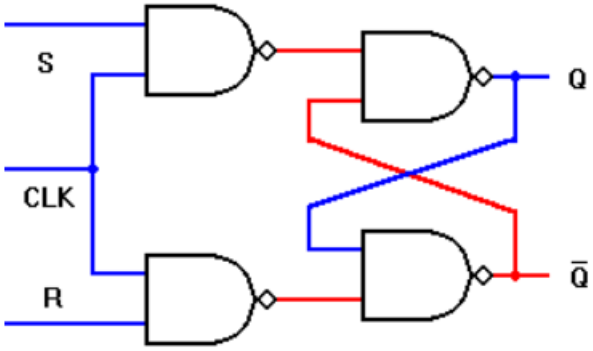
S	R	Q	$\overline{Q}$
0	0	No change	
0	1	1	0
1	0	0	1
1	1	X	X
		(Invalid)	

To analyze the circuit of S-R Flip-flop Based on NOR Gates, we have to consider the fact that the output of a NOR gate is 0 if any of the inputs are 1, irrespective of the other input. The output is 1 only if all of the inputs are 0.

Clocked S-R Flip-Flop

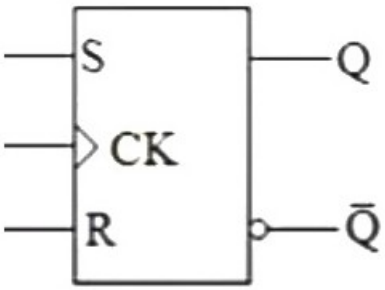
Generally, synchronous circuits change their states only when clock pulses are present. The operation of the basic flip-flop can be modified by including an additional input to control the behavior of the circuit.

When a clock pulse is used as the control signal the inputs R and S may be clocked (entered) into the flip-flop by a set of NAND gates . Such a circuit is shown below:-



The circuit shown above consists of two NAND gates. The clock input is connected to both of the NAND gates. The obvious advantage of this clocked SR flip-flop is that the inputs R and S are considered only when the clock pulse is high. As before the condition R = S = 1 is indeterminate and should be avoided.

The truth table for the Clocked R-S flip-flop is given in the table below.

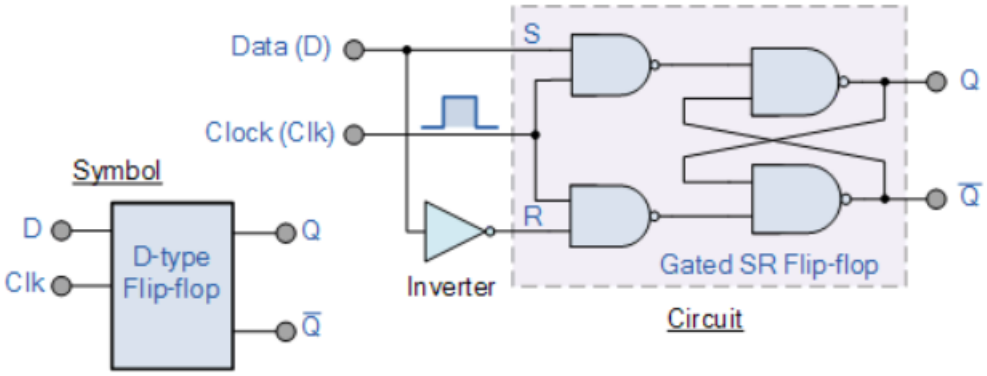


S	R	Q	$\bar{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	X	X
		(Invalid)	

One way to eliminate the undesirable condition of the indeterminate state in the SR latch is to ensure that inputs S and R are never equal to 1 at the same time. This is done in the D latch.

D Flip Flop

The D-type (Data or delay) flip flop are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input in addition to the clock input as shown in figure below. If this data input is held HIGH the flip flop would be "SET" and when it is LOW the flip flop would change and become "RESET".



The D flip-flop is either used as a delay device or as a latch to store one bit of binary information. The truth table of D flip-flop is given in the table below.

Clk	D	Q		Description
↓ » 0	X	Q	$\overline{Q}$	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Note that: ↓ and ↑ indicates direction of clock pulse