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FPGA Design of Image Encryption and Decryption Using Chua's Chaotic Masking and Artificial Neural Network

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Show details



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Abstract en

Image encryption is an important issue in protecting the content of images and in the area of information security. This article presents a two methods of image encryption and decryption one of simple and efficient masking technique based on Chua chaotic system synchronization it includes feeding the masked signal back to the master system and using it to drive the slave system for synchronization purposes. To achieve synchronization, the pecora-carroll identical cascading synchronization approach was used. The transmitted signal should be mixed or masked with a chaotic carrier and can be processed by the receiver without any distortion or loss. The other method a novel technique for image encryption and decryption using the structure of the Artificial Neural Network (ANN)-based Chua Chaotic System (CCS). For ANN-based CCS design, a Multilayer Feed Forward Neural Network (FFNN) structure with three inputs and three outputs was created. This structure consists of one hidden layer with four neurons, each of which has a Tangent Sigmoid activation function. The training of ANN-based CCS yielded a 3.602e-13

Mean Square Error (MSE) value. After successfully training the ANN-based CCS, the design was carried out on FPGA, utilizing the ANN structure's bias and weight values as a reference. These two proposed systems were efficiently designed on a Field-Programmable Gate Array (FPGA) chip utilizing the Xilinx System Generator (XSG) tool with the IEEE-754-1985 32-bit floating-point number format. The Xilinx Vivado (2017.4) design suite was used to synthesis and test the ANN-based CCS on the FPGA. The histogram, correlation coefficient, and entropy are used to perform security analysis on various images. Finally, FPGA hardware co-simulation using a Xilinx Artix7 xc7a100t-1csg324 chip was utilized to verify that the encryption and decryption of the images were successful.

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