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A New Fractal Topologies Based on Hypercube Interconnection Network

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ABSTRACT: A parallel processing system's most crucial part is a network interconnection that links its processors. The hypercube topology has exciting features, making it an excellent option for parallel processing applications. This paper presents two innovative configurations of interconnection networks based on fractal Sierpinski and a hypercube. These are the Sierpinski Triangle Topology (STT) and Sierpinski Carpet Topology (SCT). Compared to a hypercube, the Sierpinski Triangle topology (STT) noticed a significant decrease in the number of nodes and links as large networks grew. Hence, it considers a great way to reduce costs because it uses fewer nodes and links. The average distance is also shorter, which is better. Despite it has a smaller bisection width and a more degree than a hypercube by one. The Sierpinski Carpet Topology (SCT) has the advantage of having a higher bisection width than a hypercube. That is preferable because it places a lower restriction on the difficulty of parallel algorithms. In contrast, the drawback of this topology is that it has a diameter and average distance more than a hypercube.

Keywords: Interconnection network, Hypercube, Fractal, Sierpinski Triangle, Sierpinski Carpet

1. INTRODUCTION

The multicore processor technology is the foundation of any high-performance computer system today. Multicore processors are used in everything from basic embedded systems to advanced server farms. Such multicore systems' performance depends on the interconnection network connecting these cores [1]. The need to develop parallel processing in computers has become essential, leading to the advent of newer interconnection networks to enable parallel processing. Interconnection networks, abbreviated as (Ins), may be classified as either dynamic or static [2].

Connections in a static network are permanent ties, but connections in a dynamic network may be built up on the fly according to the system's requirements. Point-to-point connections directly link a processor and other processors in static networks. It is also possible to classify it further according to the connectivity pattern as either having one dimension (1D), two dimensions (2D), or a hypercube (HC). In contrast, according to the interconnection methods, dynamic networks may be divided into bus-based and switch-based categories. Two subcategories may be applied to bus-based networks: single buses and multiple buses. According to the nature of the interconnection network, switch-based dynamic networks may be classified as single-stage (SS), multistage (MS), or crossbar networks [1, 3]. The primary categories of interconnection networks display in Fig. 1.

Interconnection networks may also be divided into electrical and optoelectronic communication channels connecting processors. Examples are hypercube, mesh, ring, tree, and other electronic connectivity networks. Optical Chained-Cubic Tree (OCCT) and Optical Transpose Interconnection System (OTIS) are examples of optoelectronic interconnection networks. For OTIS, there are several architectures, including OTIS Hyper Hexa-Cell (OHHC), OTIS-Hypercube, OTIS Mesh, and many more [4].

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