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A Fifteen Levels Inverter with A Lower Number of Devices and Higher Performance

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Abstract
Multi-level inverters, as a result of the significant contributions they have made to the fields of high voltage and renewable energy applications, MLI has earned a prestigious place in the field of industrial electronics applications. The use of MLI makes it possible to generate an alternating voltage from a DC voltage or from voltages that are continuously applied thanks to this capability. The quality of the produced wave depends on minimizing the level of total harmonic distortion (THD) in the ensuing output voltage. Increasing the total number of levels is required in order to bring down the THD. The bigger the number of layers, the lower the THD. On the other hand, this necessitates an increase in the number of power switches that are utilized, in addition to an increase in the number of DC sources for certain types. A greater number of levels are achieved in this work with a reduced number of switches, and the DC source necessitates the use of specialized control over the switches as well as the grading of the DC source values. In order to demonstrate that the suggested converter achieves the needed outcomes, the MATLAB simulator is utilized.

KEYWORDS: Inverter, Multi-level inverters, THD reduction, SPWM.

I. INTRODUCTION

Multilevel inverters are commonly used today because of their voltage operation and functional versatility. The output is generated by a multilayer inverter, which draws power from many DC sources. With an increasing number of DC sources and a constant switching frequency, the inverter's voltage output waveform can be made to seem almost sinusoidal [1]-[4].

The optimal performance of the vast majority of electrical applications can be ensured by utilizing a supply that generates a sinusoidal waveform. The output voltage gets closer to having the shape of a sinusoidal wave as the number of inverter levels gets higher, which results in a decrease in the amount of total harmonic distortion (THD).

The multi-level inverter has a number of advantages over the hard-switched, two-level pulse width modulation (PWM) inverter. These benefits include a decreased dv/dt during high power operations as well as an increase in efficiency [5]-[8].

Three main types of topologies are used for multi-level inverters: cascade, diode clamp, and capacitor clamp. Cascade is the most common topology. The following topologies are included in this category: The cascade multi-level inverter is the one that requires the least amount of work to put together and has the fewest number of individual parts.

Most of the time, a cascade MLI is built using a series of DC sources and switches that are sequentially connected to one another [9]-[11].

To get the fundamental voltage and get rid of the higher-order harmonics in the output, the switches have to be turned on and off repeatedly so that alternating current voltage can be generated with several levels. This is necessary to accomplish [12].

Several DC sources contribute to its reduced switching losses and stress on the voltage supply. Multilevel inverters continue to be implemented in a growing number of facilities because of their low EMI output, high efficiency, and low switching losses in addition to their high voltage operation capacity.

Multiple levels are represented by the inverter's first three settings [13]. Multilevel inverters are becoming more common in power electronic applications as a result of the higher requirements for power quality and power rating

associated with less harmonic distortion and less electromagnetic interference.

There are a number of benefits to using a multilevel inverter for high switching frequency pulse width modulation (PWM) as opposed to a traditional two-level inverter [14-15].

The following are some of the more appealing aspects of a multilayer inverter:

- Low distortion and dv/dt stress can be used to generate the output voltage.
- The input current has a minimal distortion.
- The common mode voltage is really low.
- It has a low switching frequency.

Power switching devices and capacitor voltage sources are the structural backbone of multilevel inverters.

Due to their capacity to measure output voltage with greater harmonics, high voltages can be achieved with the maximum device rating, making them suited for high-voltage applications and voltage waveforms.

In this paper, a 15-level inverter has been suggested. The suggested multilevel inverter employs fewer switches, is more efficient, and generates fewer losses. Pulse width modulation (PWM) techniques are now widely used due to their low processing requirements, simplicity, and resilience.

The firing pulses for the switching devices are used in a particular PWM technique described in this research to produce a 15-level output voltage. As a reference, one sine waveform source is used in this procedure.

II. Circuit Description of Proposed 15-Level Inverter

Figure 1 shows the 15-level inverter. The circuit composed of H-Bridge devices with a three DC sources (V1, V2, and V3). Each source connected to the circuit through a switching device (S5, S6, and S7).

In order to understand the operation of the circuit, the operation mode for each output level is describe as following, and since they will be repeated for the remaining modes, just the first seven modes of operation will be detailed for the positive half cycle:

1- LEVEL 0 (S1 S4 =ON)
2- LEVEL 1 (S1 S4 S5 =ON)
3- LEVEL 2 (S1 S4 S6 =ON)
4- L3V3L 3 (S1 S4 S5 S6 =ON)
5- LEVEL 4 (S1 S4 S7 =ON)
6- LEVEL 5 (S1 S4 S5 S7=ON)
7- LEVEL 6 (S1 S4 S6 S7 =ON)
8- LEVEL 7 (S1 S4 S5 S6 S7 =ON)
9- LEVEL 8 (S2 S3 S5 =ON)
10- LEVEL 9 (S2 S3 S6 =ON)
11- LEVEL 10 (S2 S3 S5 S6 =ON)
12- LEVEL 11 (S2 S3 S7 =ON)
13- LEVEL 12 (S2 S3 S5 S7 =ON)
14- LEVEL 13 (S2 S3 S6 S7 =ON)
15- LEVEL 14 (S2 S3 S5 S6 S7=ON)

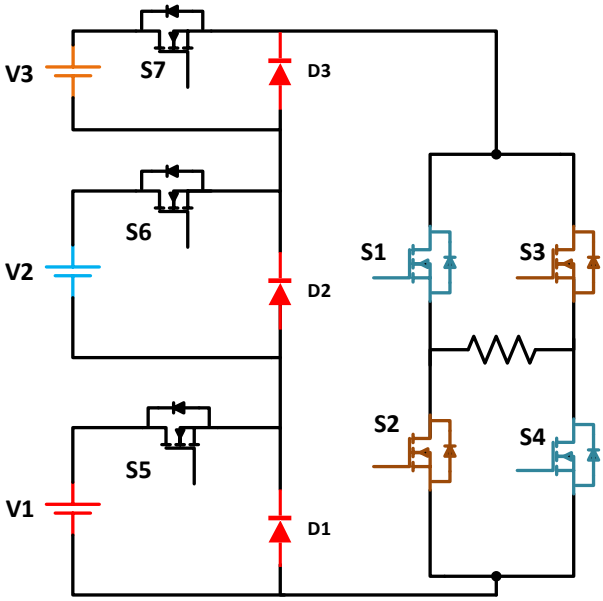

Fig. 1: The circuit diagram of the 15-level inverter.

III. The Proposed Inverter's Simulation Model & Result

Figure 2 shows the *Matlab-Simulink* model of the proposed inverter, and Fig.3 shows the control circuit of the proposed inverter. Fig.4 shows the timing pulses for the switching devices of the inverter.

This multilevel inverter has three different DC sources to choose from. The voltage that is necessary for each switch can be obtained from its own source. Where, V1=10V, V2=20V, V3=40 V leading to maximum voltage up to 70 Volt. The inverter consists of 3 front end devices (S5-S7) which are connected with a three DC voltage sources.

Using a conventional sinusoidal pulse width modulation, the H-bridge circuit's diagonal switches receive the switching pulses in order to perform their function. When one pair of the diagonal switches is turned on, the other switches are turned off, and vice versa. When S1 and S4 are turned on, the positive half of the waveform is produced, while S2 and S3 produce the negative half of the waveform.

The gate signals for the switches are generated by comparing a 3-phase, (12250 Hz) triangular-carrier signal to a (50 Hz) sinusoidal reference signal in the control circuit. The pulse width modulation approach is used for this.

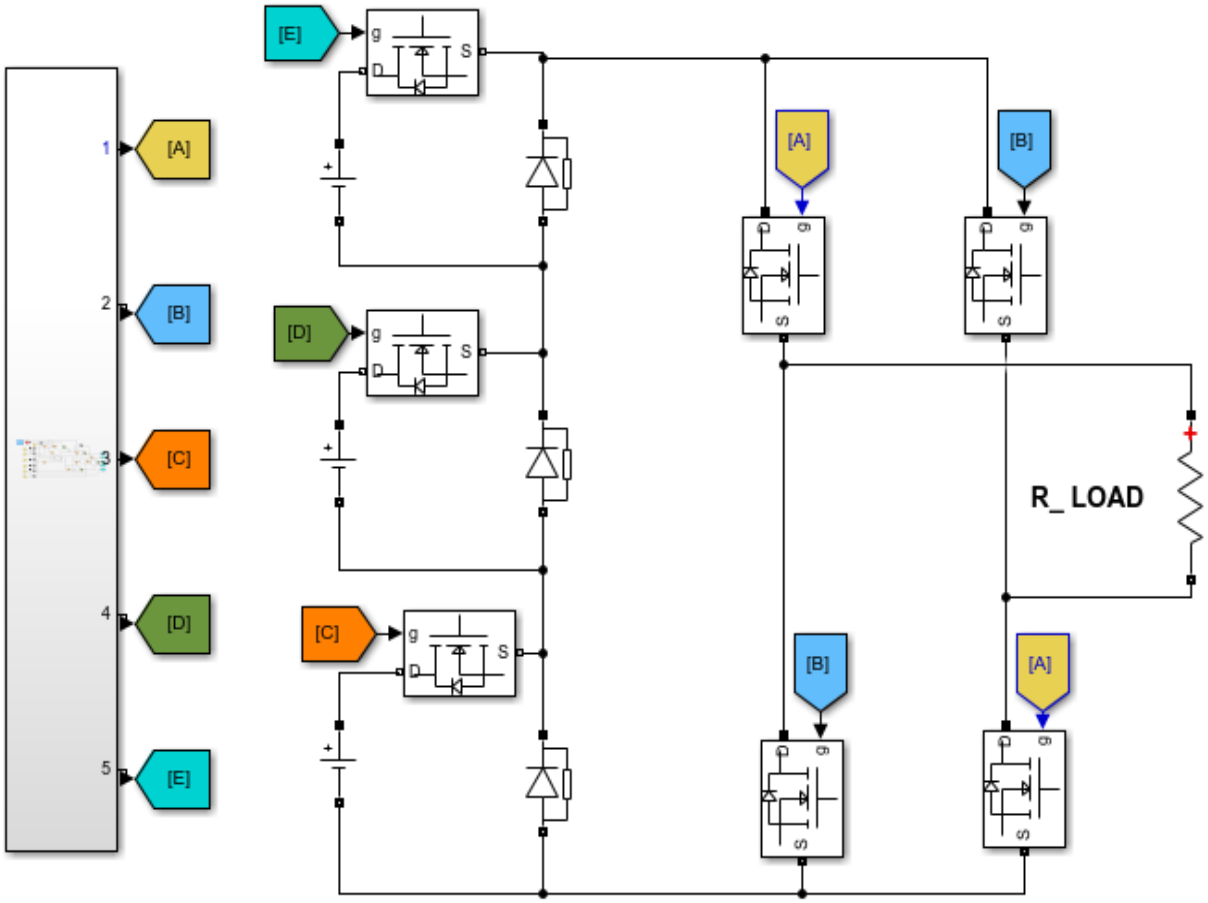

Fig. 2: The Simulink model of the proposed circuit.

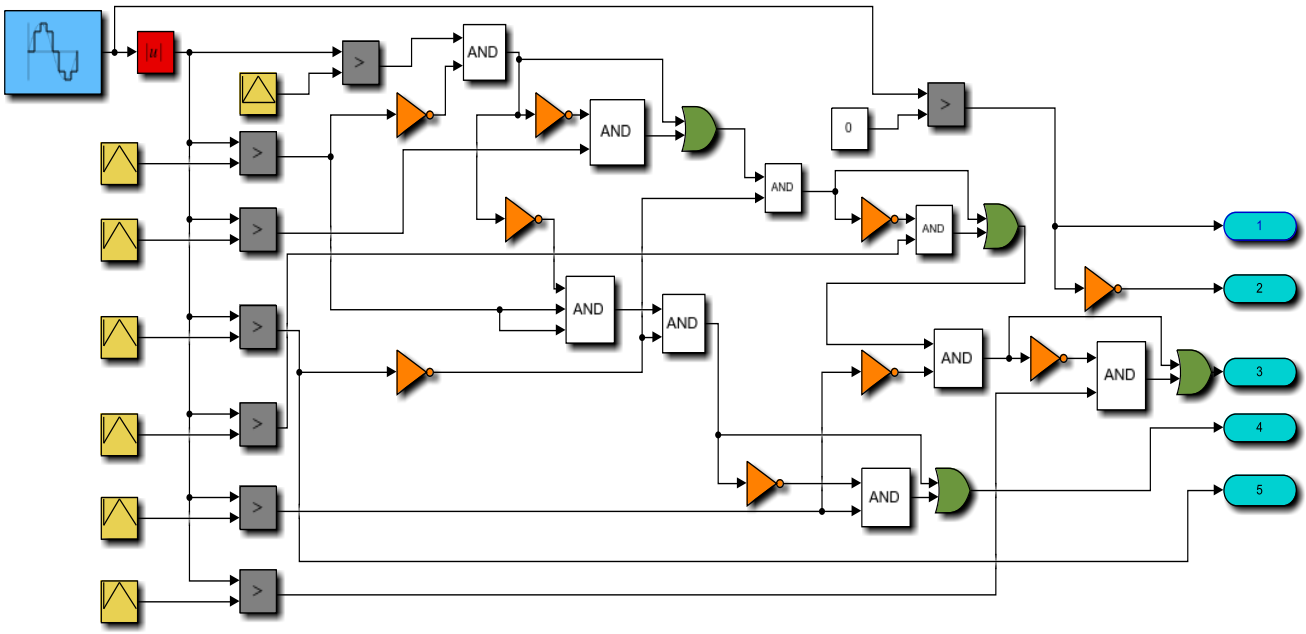

Fig. 3: The control circuit of the 15-level inverter.

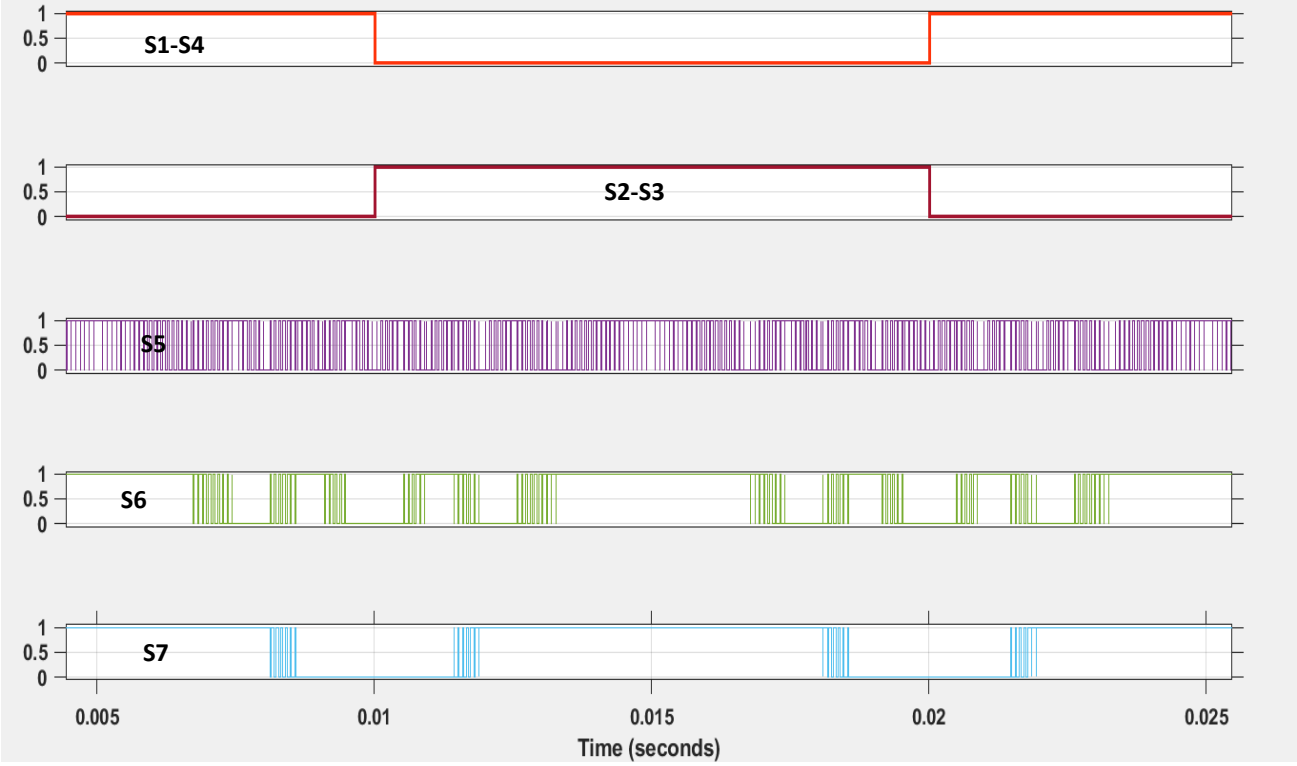

Fig. 4: The Timing signals of the control circuit.

The circuit controller is made up of a variety of logical and mathematical MATLAB functions, and it is these functions that are responsible for producing the pulses to control the proposed inverter.

Figure 5 depicts the output voltage of the inverter with 15 levels that has been proposed. Figure 6 illustrates the total harmonic distortion, or THD, that is present in the output voltage. Examining the diagram, one can observe that the THD equal to 8.24 when the modulation index m is about 0.95.

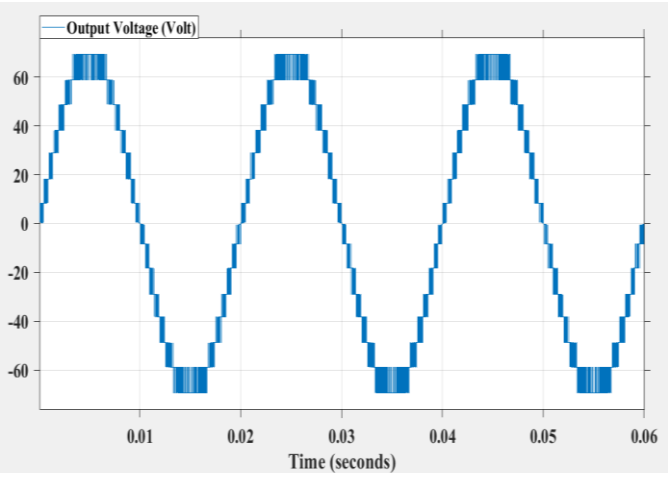

Fig. 5: The 15-level inverter output voltage.

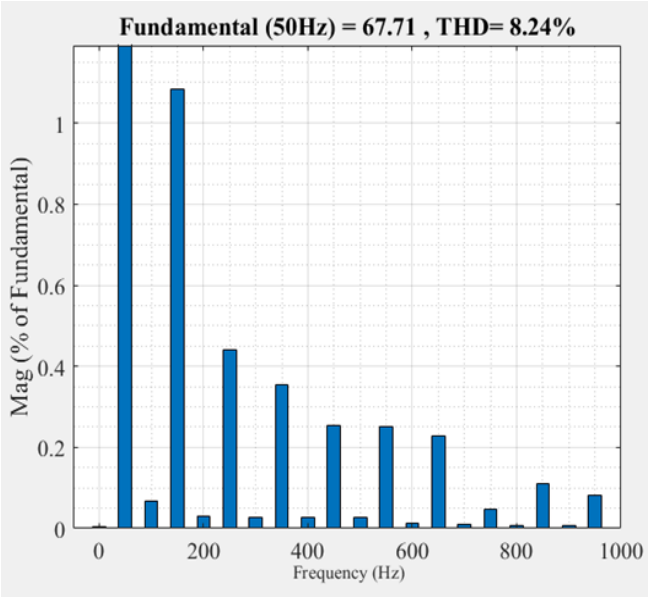

Fig. 6: The total harmonic distortion (THD) of the 15-level inverter.

IV. Conclusion

Multi-level inverters are becoming increasingly significant in today's applications. A 15-level inverter is presented in this work. The proposed inverter may produce a high-quality output voltage while minimizing overall harmonic distortion (THD). In terms of performance, it

outperforms the traditional cascaded multilevel inverter. Using the suggested control strategy, a 15-level output voltage produced with lower THD. The simulation findings show that the new configuration is more effective than the inverters that were previously employed.

CONFLICT OF INTEREST

The authors have no conflict of relevant interest to this article.

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