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Non-conventional Cascade Multilevel Inverter with Lower Number of Switches by Using Multilevel PWM

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Abstract

The multilevel inverter is attracting the specialist in medium and high voltage applications, among its types, the cascade H bridge Multi-Level Inverter (MLI), commonly used for high power and high voltage applications. The main advantage of the conventional cascade (MLI) is generated a large number of output voltage levels but it demands a large number of components that produce complexity in the control circuit, and high cost. Along these lines, this paper presents a brief about the non-conventional cascade multilevel topologies that can produce a high number of output voltage levels with the least components. The non-conventional cascade (MLI) in this paper was built to reduce the number of switches, simplify the circuit configuration, uncomplicated control, and minimize the system cost. Besides, it reduces THD and increases efficiency. Two topologies of non-conventional cascade MLI three phase, the Nine level and Seventeen level are presented. The PWM technique is used to control the switches. The simulation results show a better performance for both topologies. THD, the power loss and the efficiency of the two topologies are calculated and drawn to the different values of the Modulation index (m_a).

KEYWORDS: multilevel inverter, non-conventional Cascade inverters, HPWM.

I. INTRODUCTION

Recently, the development of the multilevel inverter has caused a great evolution in industrial applications and has increased the attention in medium and high power applications in past years [1-3].

The multilevel inverter is the power electronic system that produces desired output voltage from a few input DC sources; it can generate many voltage levels that cause harmonic content improvement, decrease the switching losses and improve the efficiency [4-5].

In general, a multilevel inverter can be divided into three groups:

(a) Diode clamped multilevel inverter type; the number of diodes is high for the high number of voltage level [6-7].
(b) Flying capacitor multilevel inverter type, the balance of the capacitor's voltage is difficult, and in the high voltage levels need a high number of capacitors [8-9].
(c) Cascade H bridge multilevel inverter type is better typology compared to the other two classic typologies. This type consists of several cells are connected in series and each cell needs DC voltage [10-12].

Cascade H bridge' type is the focus of the debate here which is divided into two groups: symmetric and asymmetric. The first type of symmetric cascade is the multilevel inverter which has an equal value of all DC voltage sources while asymmetric cascade multilevel inverter is not equal to the value DC voltage source [13,14]. The higher the output voltage level in the multi-level inverter improves the power quality; therefore, the increase in the number of levels leads to an increase in the cost, the complexity of the system, and difficulty in controlling due to the increase in the number of separate DC voltage source to control each cell and the increase in the number of switches. To overcome these problems, many proposed topologies are presented for symmetrical and asymmetrical MLI. The main advantage of all these structures is reduced the number of DC sources and the number of switches.

The proposed topology in [15] is greatly shorthand in the number of DC voltage sources and the number of switches. To produce seven-level, one H-bridge, two switches, and one DC source can be used, but in conventional cascade to produce the same number of level you need three H-bridge. It is clear that every one of H- bridge needs DC source to supply the switches can be extended the topology to generate 31 level and 127 level, also in [16] the topology is presented the similar concept by decreasing number of components and it compared with present topologies in [17].

In this paper, there are two proposed topologies for cascade multilevel with a lower number of switches with utilization pulse width modulation (PWM) control to gate switches. From the first topology, 9 levels of output voltage can be obtained while in the second topology, 17 levels can be obtained. THD, modulation index (m_a), power losses, and efficiency can be obtained for each type and the results are compared with the conventional cascade multilevel inverter.

II. Conventional CASCADE H BRIDGE

One type of multilevel inverter consists of a DC source within H- bridge cells which are connected in series. Each cell is supplied by an individual DC source and consists of two branches that are connected in parallel, and each branch contains two switches (one is complementary to the other). The same arrangement in the second branch is applied for the switches.

The output voltage consists of levels that depend on the number of cells, Fig.(1) is illustrated a single cell, it is given three levels $-V_{dc}$, 0, V_{dc}. To provide a high level of output voltage, the number of cells must be increased, the number of levels (m) becomes [18]:

$$m = 2n + 1 \quad (1)$$

Where n is the number of H -bridge.

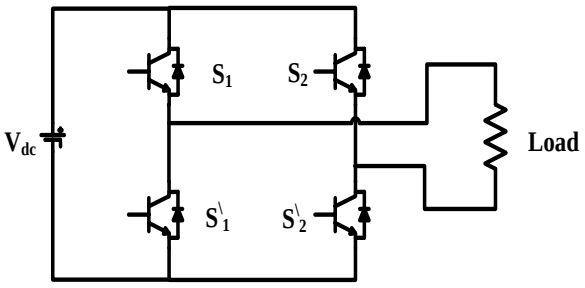


Figure (1): single cell conventional cascade three level

III. Multi PWM Technique and Hybrid PWM

The most common control technique for traditional inverters is the pulse width modulation (PWM) method. The popularity is due to its simplicity and good result, and it guarantees all operating conditions. In addition, it can be implemented easily for MLIs. For using m-level inverter, (m-1) carrier signals with the same amplitude and frequency are needed. The principle of PWM is the switching signals which are generated [19,20].

Hybrid PWM (HPWM) can be described by adding a zero sequence component to the three-phase modulating signal to avoid over-modulation. These are represented as:

$$V_a^{**} = V_a^* + V_{zs}^* \quad (2)$$
$$V_b^{**} = V_b^* + V_{zs}^* \quad (3)$$
$$V_c^{**} = V_c^* + V_{zs}^* \quad (4)$$

where ($V_a^{**}, V_b^{**}, V_c^{**}$) represent the input reference voltage which compared to the carrier signals, (V_a^*, V_b^*, V_c^*) represent the sinusoidal voltages for phase a, b and c have phase shift is 0,-120, and 120 respectively

V_{ZS}^* is the zero sequence voltage describe by the equation:

$$V_{ZS}^* = [(1 - 2K_o) + K_o Va^* + (1 - 2K_o)Vc^*] \quad (5)$$

Where $0 \leq K_0 \leq 1$ is the factor either constant or variable and this factor affects the voltage wave [21].

IV. Non-conventional cascade Nine levels proposed topology

Figure (2) represents one phase of nine level inverter with a reduced number of switches [22], it contains two parts level marker part and H- bridge part. The level marker part consists of seven switches and four DC sources. When the DC source and switches are arranged, voltage levels are produced but the polarity of the output voltage is limited by the H-bridge part.

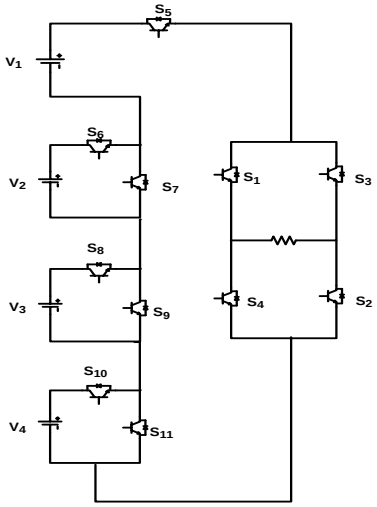


Figure (2): one phase non-conventional cascade 9- Level

The switches (S_6, S_8, S_{10}) and (S_7, S_9, S_{11}) are complements respectively. H bridge is utilized to change the polarity of the switches (S_1, S_2) which are operated in the positive half cycle while the switches (S_3, S_4) are operated at negative half cycle. This topology contains the switches which are less than the conventional cascade nine levels which contain four of H bridge, also this topology can be extended to a high level of the output voltage based on the following equations :

$$N_{level} = 2n + 1 \quad (6)$$
$$N_{switch} = 2n + 3 \quad (7)$$
$$V_{o_{max}} = 2n \quad (8)$$

Where n is the number of DC sources.

N_{level} is the number of output voltage levels.

N_{switch} denote the number of switches.

And Vo_{max} is the maximum output voltage.

In this paper, PWM is used as a control to gate the switches by comparing the reference wave (rectified sine wave) with four carriers (triangular wave) for time intervals which illustrate in Fig. (3).

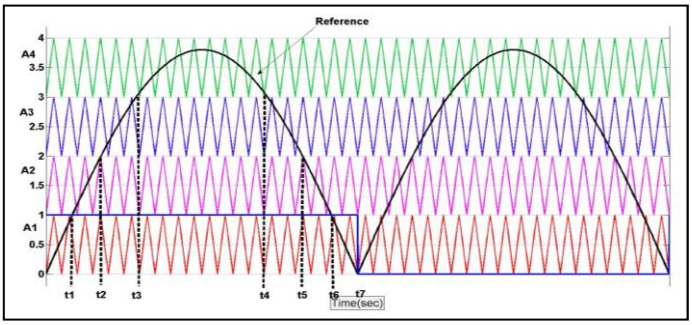


Figure (3): PWM control method used for 9-level cascade

The operation of the circuit represents four modes depending on time interval as follows:

Mode (1) time interval $0 < t < t_1$ & $t_6 < t < t_7$ in Fig.(3)

From time interval from 0 to t_1 the switch (S_5) is turned ON when the reference waveform (/A_m sinwt/) is higher than the first carrier which has amplitude (A_1) and the switches (S_6, S_8, S_{10}) remain OFF state in this interval but (S_7, S_9, S_{11}) are turned ON because these switches are complement with switches (S_6, S_8, S_{10}) respectively, then the output voltage $V_{out} = V_1$, (S_1, S_2) are turning ON during positive half cycle as shown in Fig. (4-a) below.

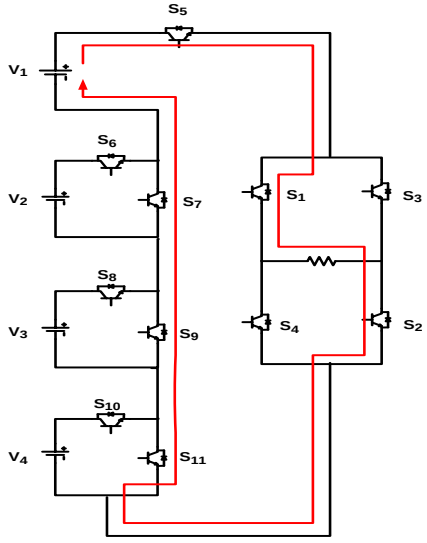


Figure (4-a): Mode (1) Operation of Circuit

Mode (2) time interval $t_1 < t < t_2$ & $t_5 < t < t_6$ in Fig. (3)

The switch (S_6) is turned ON for time interval from t_1 to t_2 when the reference wave (/A_m sinwt/) is compared with the second carrier which has amplitude (A_2) and remains (S_5) is turned ON from mode (1) but other switches (S_8, S_{10}) are kept OFF the output voltage $V_{out} = V_1 + V_2$ and when (S_6) is turned OFF the output voltage $V_{out} = V_1$ this operation will be repeated for the time interval from t_5 to t_6 as shown in Fig.(4-b).

Mode (3) time interval $t_2 < t < t_3$ & $t_4 < t < t_5$ in Fig. (3)

For time interval between t_2 and t_3 the switch (S_8) is switched ON and stay with switches (S_5, S_6) are turned ON produced output voltage $V_{out} = V_1 + V_2 + V_3$ and when the switch (S_8) is OFF then the output voltage will be $V_{out} = V_1 + V_2$, the same output voltage levels are obtained at time interval from t_4 to t_5 as shown in Fig. (4-c)

Mode (4) time interval $t_3 < t < t_4$ in Fig. (3)

The switch (S_{10}) is turned ON and keeps the switches (S_5, S_6, S_8) ON so complement switches are in the state OFF then the output voltage is obtained $V_{out} = V_1 + V_2 + V_3 + V_4$ as shown in Fig. (4-d).

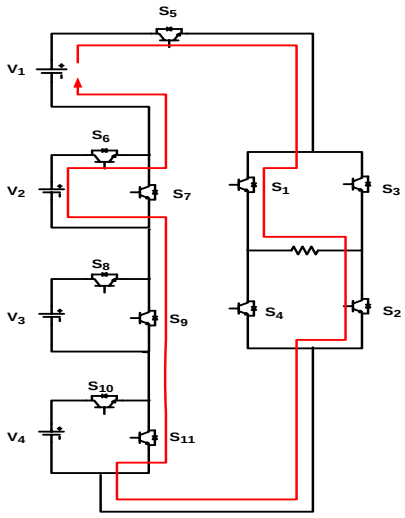


Figure (4-b): Mode (2) operation of the circuit

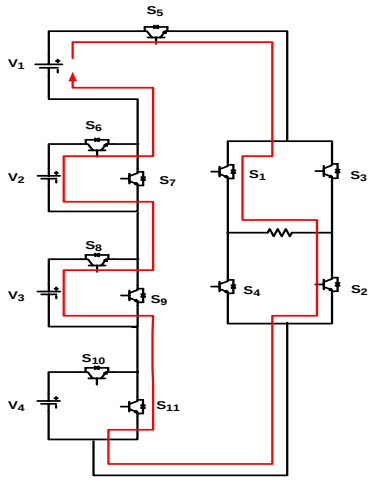


Figure (4-c): Mode (3) operation of the circuit

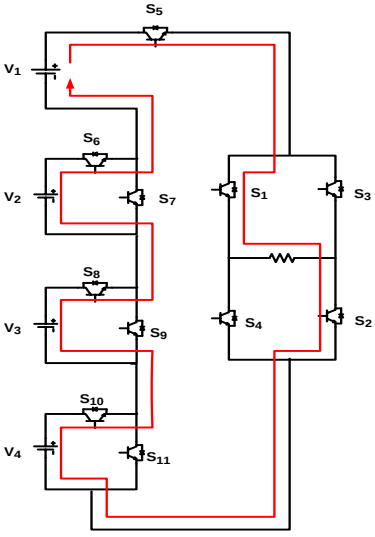


Figure (4-d): Mode (4) operation of the circuit

The negative levels are obtained when the switches (S_3, S_4) are turned ON and the modulating signal (reference wave) is compared with carrier signals (triangular wave) in the reverse period.

V. Simulation Results of Non-Conventional 9-Level Cascade MLI

The simulation is performed for three phase cascade 9-level for phase a contain the switch (S_5) and the switches (S_6, S_8, and S_{10}) are complements with switches (S_7, S_9, and S_{11}) respectively, the switches (S_1 and S_2) are operated during positive half cycle while (S_3 and S_4) are operated during the negative half cycle and four DC source have values of 200V and resistance load has value of 15 ohm. The circuit of the non-conventional cascade is in three phases and is operated at modulation index 0.5 and the switching frequency 18000HZ. At these values, the less value of THD is obtained.

To clarify how to control the switches, Fig. (5) illustrates the simulation of the comparison between rectified sinewave with modulation index 0.5 and frequency index 18000/50 with a triangular wave.

The firing pulse generation of phase a is shown in Fig. (5), the first carrier in phase a with an amplitude (A_1) is used to control the switch (S_5) while the switch (S_6) and its complement (switch (S_7)) are controlled by the comparison between rectified waveform and second carrier with an amplitude (A_2). The same way for controlling the switch (S_8) and its complement (switch (S_9)) are controlled by the comparison between rectified waveform and third carrier with an amplitude (A_3). For controlling (S_{10}) and (S_{11}) the fourth carrier (A_4) is used.

The pulse generator with a pulse width of 50% of a period can be used to control H- bridge circuit. The same circuit can be used for phase b and phase c but shifting reference by 120°, 240° respectively.

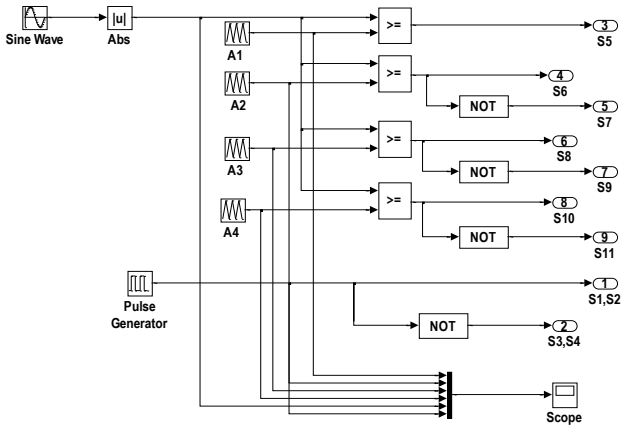
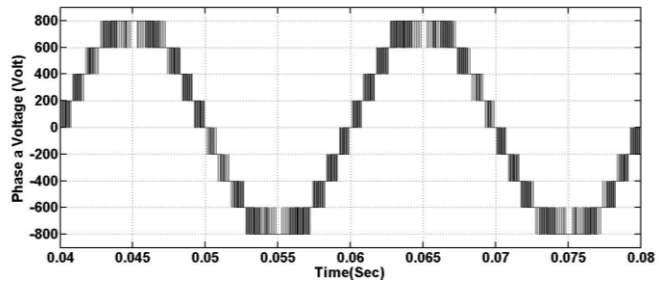
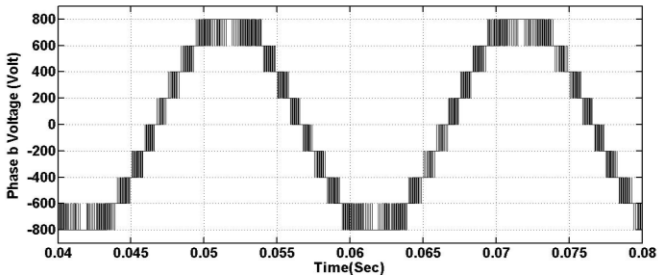


Figure (54): Firing pulse generation of switching

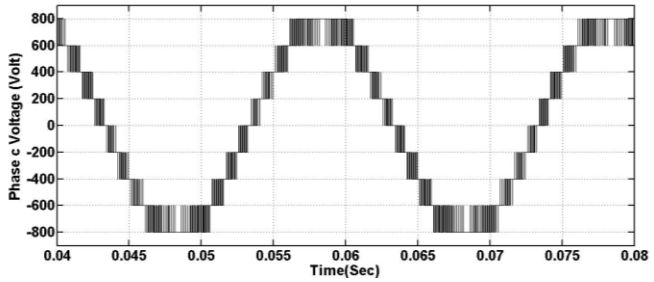
The output voltage for the 9-level MLI is shown in Fig.(6). Steps of voltage in each phase are equal to the levels of inverter and the phase shift 120° between each phase.



(a)



(b)



(c)

Figure (6): Simulations results in (a) Output Voltage of phase a.(b) Output Voltage of phase b(c) Output Voltage of phase c

THD is high in the using inverter, so the criteria of selecting the type of circuit are to minimize the THD in the output voltage. For this circuit, the minimum THD is 12.1% is obtained at switching frequency Fc=18000 Hz and modulation index 0.5, as shown in Fig.(7). The minimum value obtained from THD is still higher, therefore, to reduce the harmonic distortion in the output voltage, it is recommended to use Low Pass Filter LPF to eliminate the harmonic and get lower THD which is equal to 1.14%.

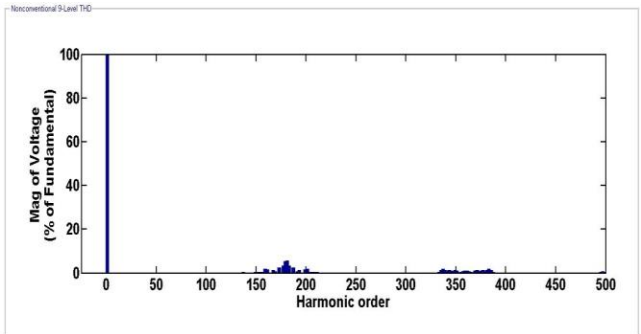
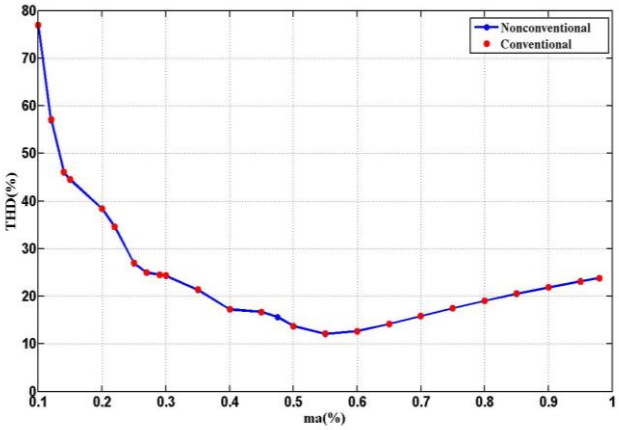


Figure (7): THD of the output voltage waveform

The basic discussion of this paper is the comparison between conventional and non-conventional MLI. The conventional cascade nine level consists of four H bridges, so four DC sources and sixteen switches are required to get nine levels in the output while the non-conventional consists of four DC sources with seven switches for the same output. Figure (8) illustrates the comparison with THD for the operation of the two circuits conventional and non-conventional cascade nine levels at different values of m_a. From this figure, it appears that THD is decreased with an increase in the values of m_a, and minimum THD is obtained at m_a equal to 0.55 and then THD is increased again.



Figure(8): Change THD with m_a for Constant Switching Frequency

At a constant modulation index as m_a=0.55, the switching frequency is changing to get different THD values and compare the performance of the two circuits. Figure (9) illustrates that THD in non-conventional is less than conventional but the value of THD for every circuit will change in small value when the values of switching frequency are changed.

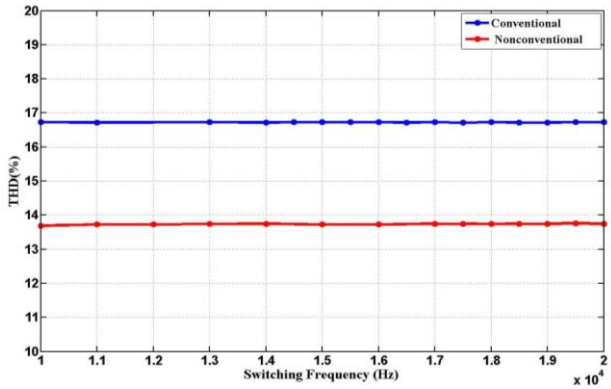
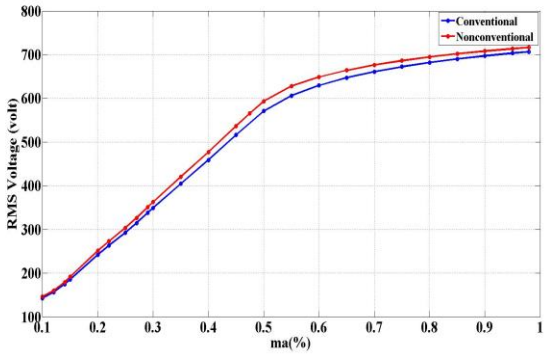


Figure (9): Change THD with Switching Frequency at m_a equal 0.5

RMS voltage increases linearity at a small value of m_a while staying constant at large values of m_a as shown in Fig. (10)



Figure(10): Change RMS voltage with m_a at Constant Switching Frequency

Losses in the circuit give an idea about the circuit behavior, so Fig. (11) represents the two circuit losses. Losses in the two circuits are almost equal but when checking, it is found that the non-conventional circuit losses are at some point less than the conventional circuit losses, while the losses for both circuits are rapidly increased for the modulation index greater than 0.6 when all switches are turned ON for the whole time.

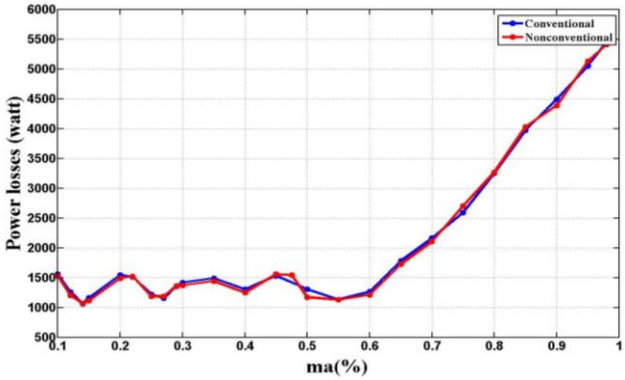


Figure (11): The Change in Power Losses with m_a at Constant Switching Frequency

Efficiency is one of the parameters used to measure the quality of the circuit, and Fig. (12) illustrates the efficiency for both conventional and non-conventional circuits, both curves seem identical but non-conventional has high efficiency in tiny value.

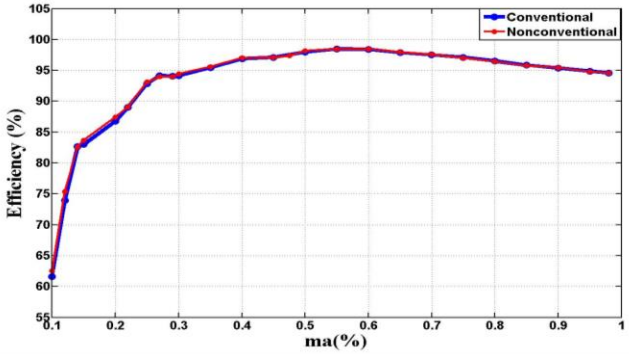


Figure (12): Comparison of the Efficiency for conventional and nonconventional nine levels at Constant Switching Frequency 18000 Hz

When the same circuit three phase non-conventional nine-level is controlled by HPWM, simulation of the controlling method is illustrated in Fig. (13) which is represented by the equations (1) to (4). A zero sequence component (Vzs^*) is added to the three-phase sinusoidal modulating signal (V_a^*, V_b^*, V_c^*) results in the inverter fundamental voltage ($V_a^{**}, V_b^{**}, V_c^{**}$) and these are the voltages that are used for comparison with carrier signals to produce pulse to gate the switches as shown in Fig. (14).

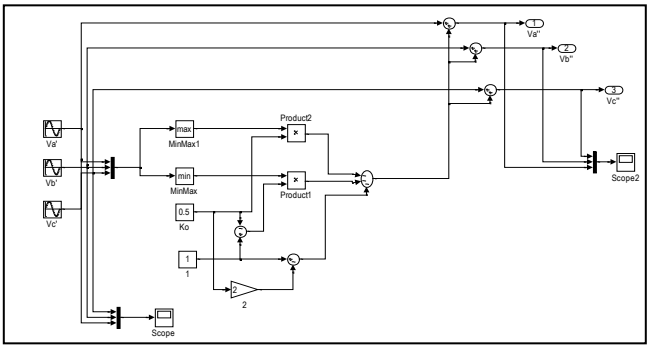


Figure (13) Simulink HPWM configuration For reference voltage

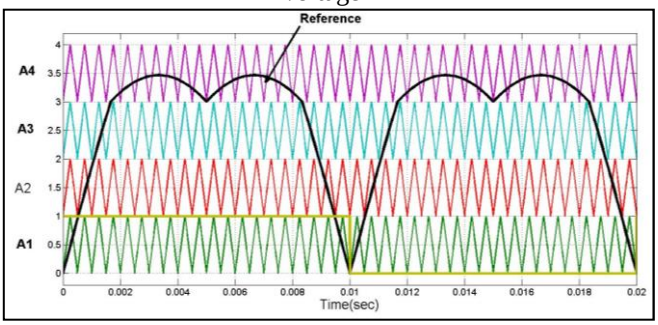


Figure (14): PWM control method for 9 levels used HPWM

Three-phase HPWM nine-level non-conventional cascade is operated at a frequency index of 18000/50 and modulation index (ma) 0.6. It appears the least value of THD is 25.75% as shown in Fig. (15), and compared with conventional HPWM nine level cascade at the same frequency index and different values of modulation index illustrate in Fig. (16).

Figure (15) represents THD for a hybrid non-conventional nine-level cascade circuit at modulation index and frequency index to get the minimum value of THD.

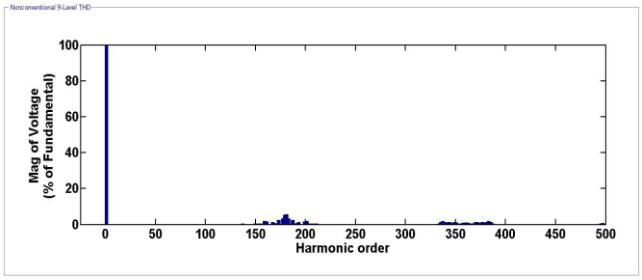


Figure (15): Harmonic content in the output voltage waveform for phase a

The THD for the two circuits conventional and non-conventional is illustrated in Fig. (16). It is clear that the non-conventional circuit has a minimum THD at a modulation index of 0.6 which is the same value as the conventional circuit.

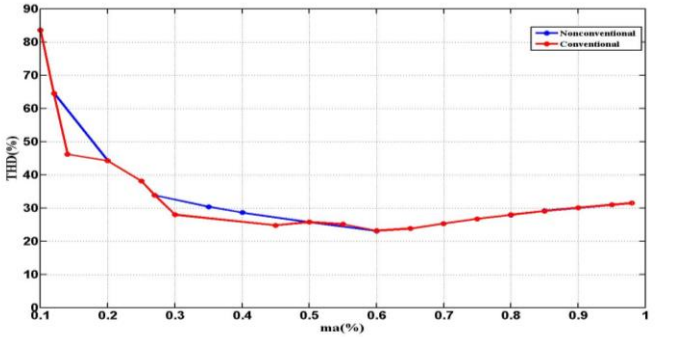


Figure (16): Simulink result comparison THD for nonconventional topologies and conventional nine levels at Constant Switching Frequency

Selecting the switching frequency for both circuits depends on the value of THD. Minimum THD has been obtained when operating both circuits at a switching frequency of 18000 Hz. Figure (17) illustrates the different values of THD at different switching frequencies for both circuits.

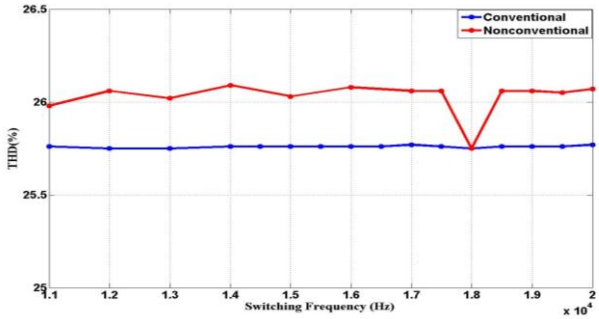


Figure (17): Simulink result ChangeTHD With Switching Frequency for conventional and nonconventional nine levels by using HPWM control

Power loss for the Hybrid circuit is shown in Fig. (18). The power losses for both circuits are almost equal with a small difference in value. The efficiency curves for both circuits are closed to each other and almost identical, maximum efficiency is 95% at a modulation index equal to 0.6 as shown in Fig. (19).

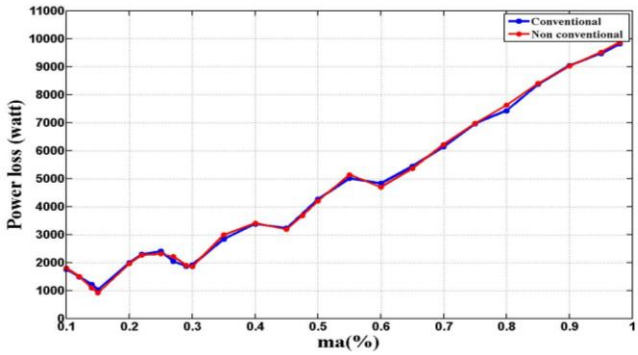


Figure (18): The simulation results of Power Loss for conventional and nonconventional nine levels at Constant Switching Frequency by using HPWM control

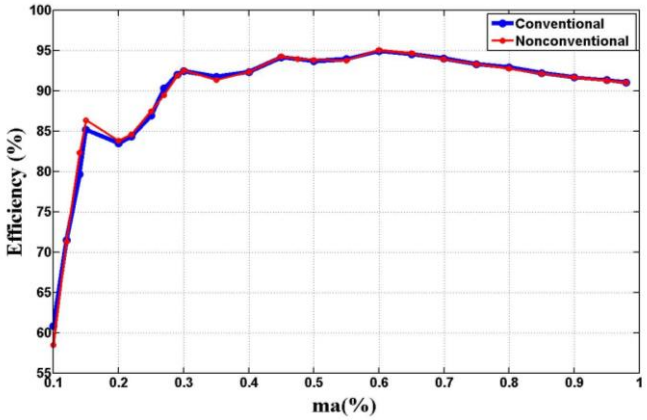


Figure (19): Change Efficiency with m_a at Constant Switching Frequency 18000 Hz by using HPWM control

The RMS voltage of the output for two circuits at different values of m_a illustrates in Fig. (20).

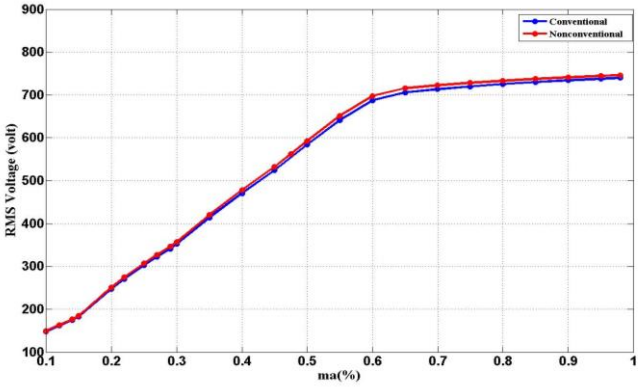


Figure (20): The change in RMS Voltage with m_a at Constant Switching Frequency 18000 Hz

VI. NON-CONVENTIONAL CASCADE SEVENTEEN LEVELS TOPOLOGY

The single cell for the topology contains eight switches and four DC sources. The operation of switches (S_5, S_7, S_9, and S_{11}) are complemented with (S_6, S_8, S_{10}, and S_{12}) illustrate in Fig.(21), and the following formula is used to extend the number of levels [23].

$$N_{switch} = 8n \quad (9)$$

$$N_{source} = 4n \quad (10)$$

Where n is the number of the basic cell n= 1,2,….

The structure is given seventeen levels for one phase by using two single cells. This topology aims to reduce the number of components. The conventional cascade seventeen levels need eight H-bridge which means 32 switches while this topology needs one H bridge and sixteen switches and the number of switches will be reduced to half of the conventional ones. Figure (21) illustrates non-conventional cascade 17 levels. The circuit of cascade 17- level consists of switches with operating philosophy as (S_5 and S_6) (S_{13} and S_{14}) are complement in the first and second basic cell as main switches to activate the cells S_5 in the first cell only can be eliminated. However, it is indicated in the configuration to preserve the basic design of cells as it is considered a standard design cell. Other switches in the same cells like (S_7 and S_8), (S_9 and S_{10}), (S_{11} and S_{12}) are complements for each other and used to activate the H- bridge within each cell to add a new level to the output. Each couple of switches are complimented for two reasons: the first one is to energize and de-energize the DC supply, while the other reason is to avoid the short circuit on the DC source. Switches (S_{15} and S_{16}), (S_{17} and S_{18}), (S_{19} and S_{20}) work in the same way for the second cell. The switches (S_1 and S_2) are turned ON during the positive half cycle while the switches (S_3 and S_4) are turned ON during the negative half cycle.

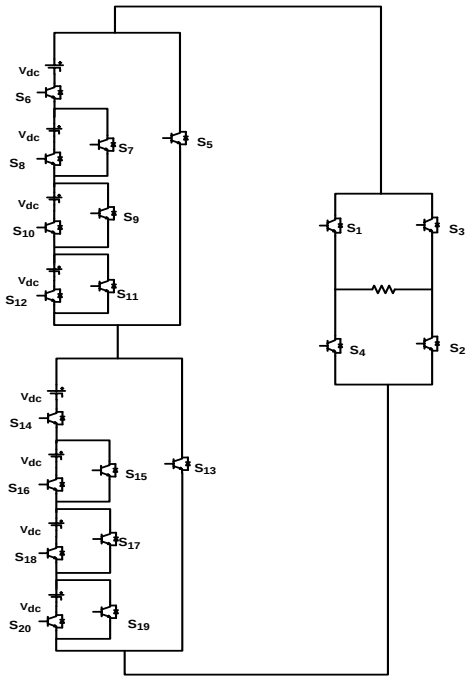


Figure (21): Basic circuit of one phase cascade 17- level

PWM technique is used for controlling the switches in this topology which uses eight triangle wave and rectified sine wave for comparison as shown in Fig. (22)

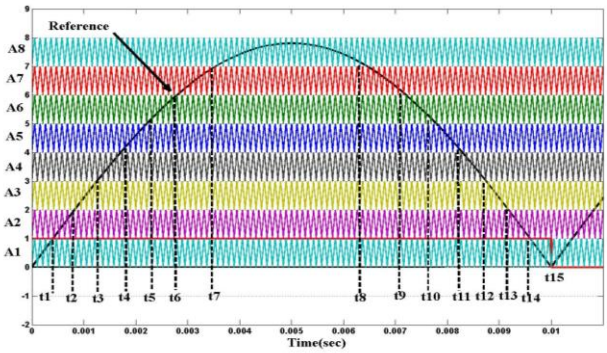


Figure (22): PWM control method used for 17-level cascade inverter

The operation of this circuit consists of eight modes as follows:

Mode (1) For time interval $0 < t < t_1$ & $t_{14} < t < t_{15}$ in Fig. (22)

In this mode, the time interval from 0 to t_1 the switch S_6 is turned ON when other switches (S_8, S_{10}, S_{12}, and S_{14}) are OFF state the output voltage $V_{out} = V_{dc}$ because (S_6, S_7, S_9, $S_{11}$and S_{13}) are turned ON but if S_6 is off state the output voltage $V_{out} = 0$ as shown in Fig. (23- a), and the switches (S_1 and S_2) are turned ON always during the positive half cycle to complete the flow of the current, the same switches operation at time interval t_{14} to t_{15}.

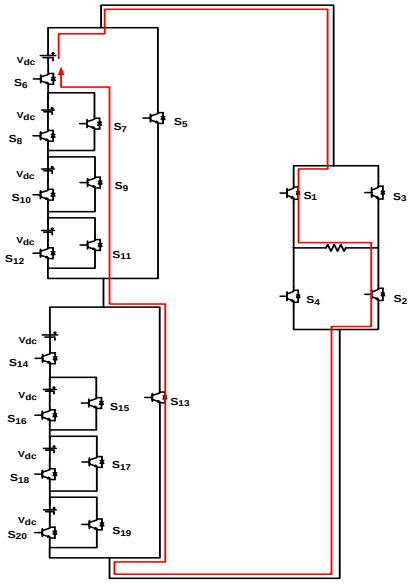


Figure (23-a): Mode (1) of circuit operation

Mode (2) for the time interval $\mathbf{t_1 < t < t_2}$ **&** $\mathbf{t_{13} < t < t_{14}}$ in Fig. (22)

For this interval, switching will be applied to switch S_8 to turn ON and OFF with its complement the While other switches (S_6, S_9, S_{11}, S_{13}) are kept ON to complete the circuit to the output voltage, $V_{out} = 2V_{dc}$ as shown in Fig. (23- b) or $V_{out} = V_{dc}$ when S_8 is OFF state/ and this operation will be repeated for time interval t_{13} to t_{14} when the reference voltage intersects with the second carrier.

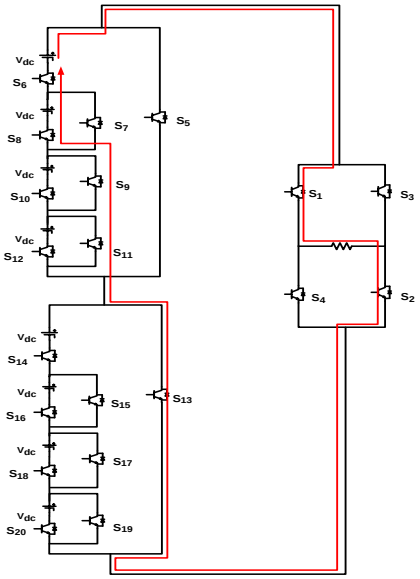


Figure (23-b): Mode (2) of circuit operation

Mode (3) for the time interval $t_2 < t < t_3$ & $t_{12} < t < t_{13}$ in Fig. (22)

In this time, the interval from t_2 to t_3 and time interval from t_{12} to t_{13} the reference voltage intersect with the third carrier to gate S_{10} and its complement, the switches (S_6 and S_8) are still ON also the switches (S_{11} and S_{13}) are turned ON the output voltage $V_{out} = 2V_{dc}$ or $3V_{dc}$ according to the status of switch S_{10} as shown in Fig. (23 - c).

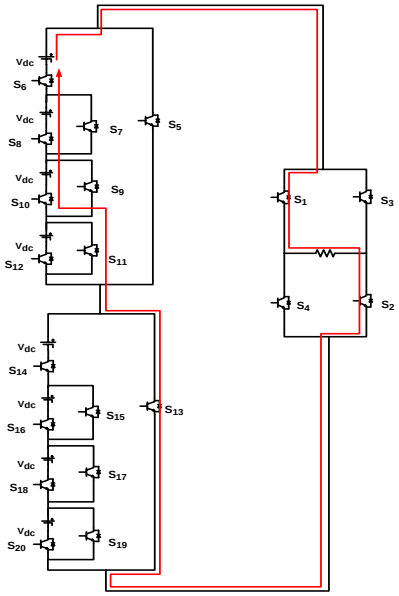


Figure (23-c): Mode (3) of circuit operation

Mode (4) For time interval $t_3 < t < t_4$ & $t_{11} < t < t_{12}$ in Fig (22)

In the time interval t_3 to t_4 and t_{11} to t_{12}, the firing circuit will ignite S_{12}, other switches (S_6, S_8, S_{10}, and S_{13}) are switched ON to apply the output voltage $V_{out} = 4\ V_{dc}$ as shown in Fig. (23 – d).

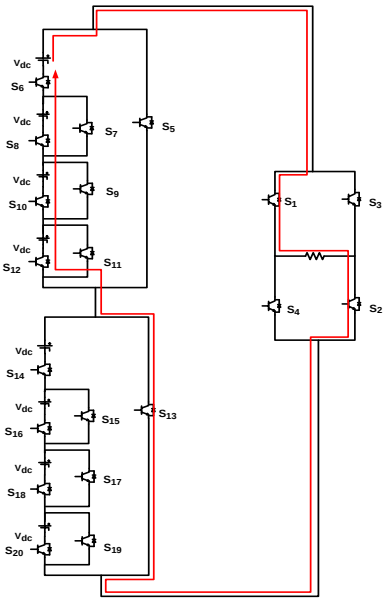


Figure (23-d): Mode (4) of circuit operation

Mode (5) For time interval $t_4 < t < t_5$ & $t_{10} < t < t_{11}$ in Fig. (22)

For this mode and all coming mode, the switches (S_6, S_8, S_{10}, and S_{12}) in the first cell will remain ON, for this period the switch S_{14} is turned ON and the other switches in the second cell (S_{15}, S_{17}, and S_{19}) are turned ON, the output voltage in a result will be $V_{out} = 4\,V_{dc}$ or $5V_{dc}$ depend on the S_{14} Status. This will be repeated for the time interval from t_{10} to t_{11} in the same operation of the switches Fig. (23-e) illustrate mode 5.

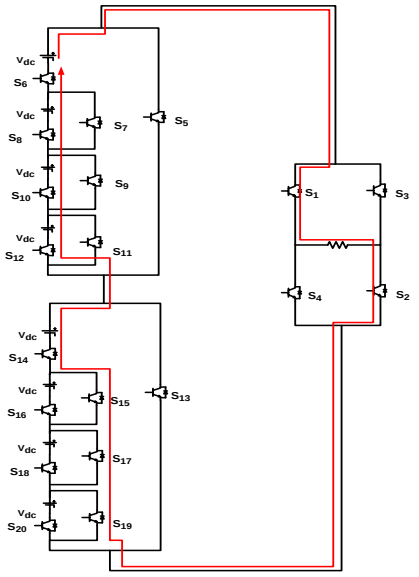


Figure (23-e): Mode (5) of circuit operation

Mode (6) for time interval $t_5 < t < t_6$ & $t_9 < t < t_{10}$ in Fig (22)

Same mode 5 the first cell will be energized, from the second cell switches (S_{14}, S_{17}, and S_{19})which are kept ON. So for this interval, the Switch S_{16} will be controlled by intersecting the reference voltage with the sixth carrier, the output voltage $V_{out} = 5V_{dc}$ or $6V_{dc}$ and the same controlling repeat for the time interval from t_9 to t_{10} as shown in Fig. (23 –f).

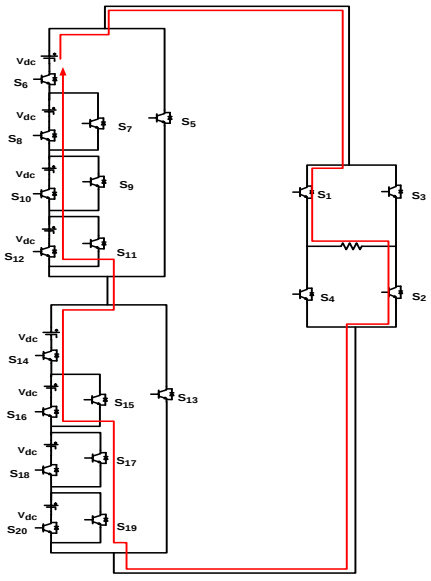


Figure (23-f): Mode (6) of circuit operation

Mode (7) for time interval $t_6 < t < t_7$ & $t_8 < t < t_9$ in Fig.(22)

First cell switches will be as Mode 5 and the switches in the second cell (S_{14}, S_{16}, and S_{19}) are turned ON while the controlling in this mode will be applied on switch S_{18} to get output voltage $V_{out} = 6V_{dc}$ or $7V_{dc}$ and the same switch is gating in the time interval t_8 to t_9 as shown in Fig. (23 –g).

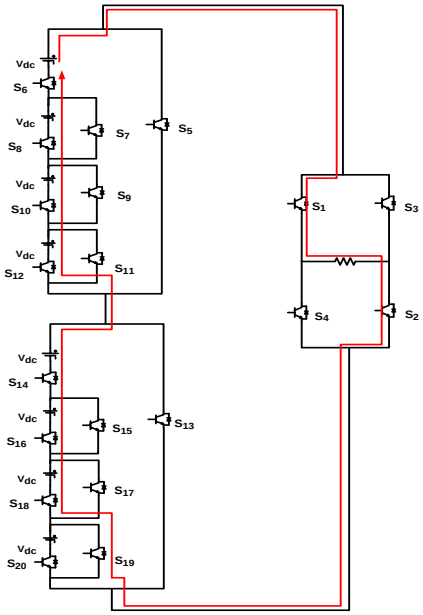


Figure (23-g): Mode (7) of circuit operation

Mode (8) for time interval $t_7 < t < t_8$ in Fig. (22)

First cell switches will be as Mode 5 and the switches in the second cell (S_{14}, S_{16}, and S_{18}) are turned ON while the controlling in this mode will be applied on switch S_{20} to get $V_{out} = 7V_{dc}$. Or $8V_{dc}$ as shown in Fig. (23 –h).

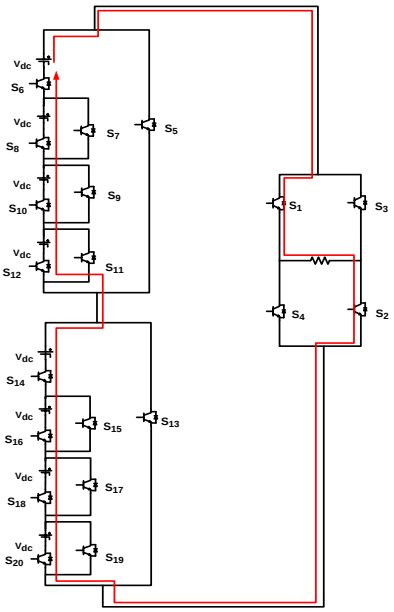


Figure (23-h): Mode (8) of circuit operation

The same method is utilized in the negative half cycle but in the reverse interval of the time and the switches (S_2 and S_3) are gating in the negative cycle.

VII. Simulation Results of Non-conventional Cascade 17-Level MLI

Figure (24) shows the Simulink for firing circuit for a single phase of the cascade 17 level. For gating switches, the PWM technique is used by comparator modulation wave with eight carrier wave at different time intervals as shown in Fig. (22). at ma = 0.5, the frequency index is 19000/50 and the DC source has a value of 200 v to feed the resistive load of 15 ohm.

This figure illustrates the simulation of controlling non-conventional cascade 17 level. It contains the comparison rectified sine wave with four carriers to control eight switches in the first basic cell and four other carriers for controlling eight switches in the second basic cell. The comparison with the first carrier is controlled (S_6) and the complement is controlled (S_5). The comparison with the second carrier is controlled (S_8) and the complement (S_{10}). The same method is repeated for other carriers to control switches, the pulse generator is used to remain the switches ($S_1$and S_2) are turned ON during the positive half cycle while the switches (S_3 and S_4) are turned ON during the negative half cycle.

The operating frequency for a non-conventional 17-level cascade circuit is chosen depending on the value of THD of the output voltage, for different values of the switching frequency, 19000 Hz is the frequency that obtained the minimum THD.

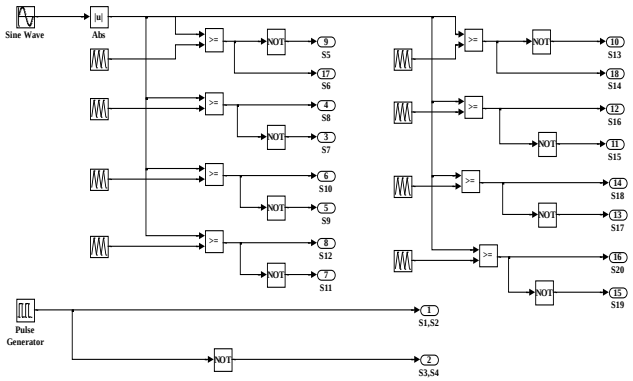
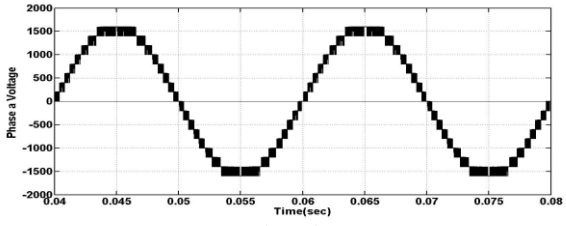
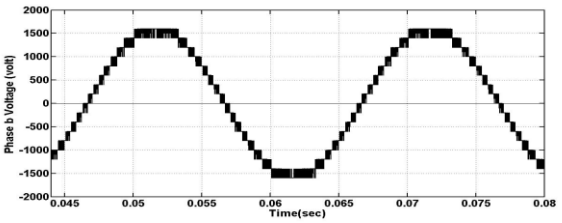


Figure (24): Firing Pulse generation of the switching

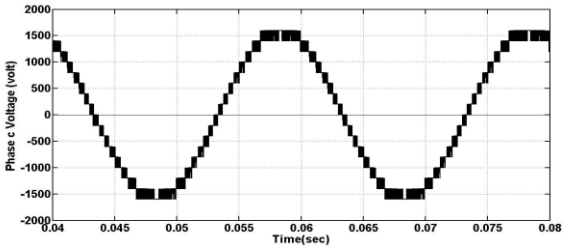
The output voltage for phase a is illustrated in Fig. (25-a), it consists of seventeen levels, and phase (b and c) have the same output levels but with phase shift -120, 120 respectively are illustrated in Fig. (25-b) and Fig. (25-c)



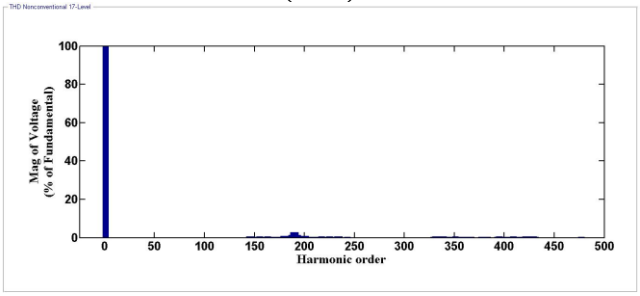
(25-a)



(25-b)



(25- c)



(25-d)

Figure (25): Simulations Results in (a) Output voltage for phase a. (b) Output voltage for phase b (c) Output voltage for phase c (d) THD of the output voltage waveform

The reason for increasing the levels is to reduce the harmonic in the output voltage, and this is clear when comparing the THD of the 17-level with the 9-level topology, THD for this circuit is 6.97% which is the best result achieved when using Low Pass Filter LPF in the output as shown in Fig. (25-d).

To compare between conventional and non-conventional, different values for THD are measured by changing the modulation index value with a constant switching frequency to obtain the lowest THD which is found at m_a= 0.5, as shown in Fig. (25).

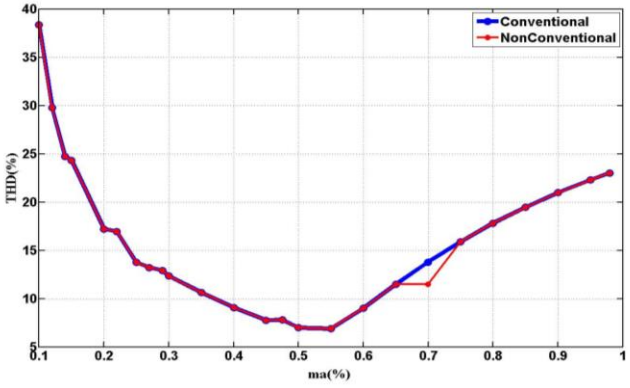


Figure (26): Change THD with m_a at Constant Switching Frequency

Figure (27) illustrates how the frequency index has been chosen and used as a constant for another Simulink result. At this frequency, the two types conventional and non-conventional are identical in the THD when the circuits are operated at the same switching frequency of 19000 Hz.

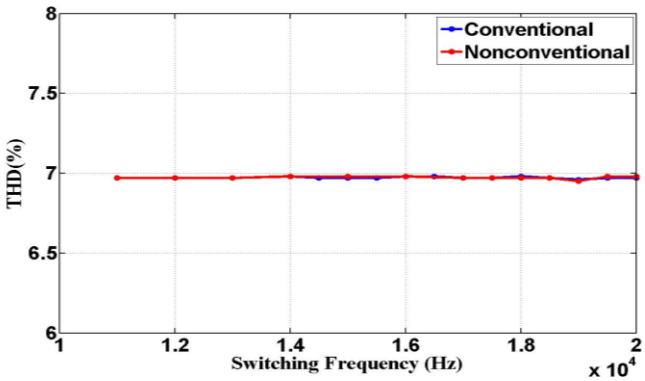


Figure (27): The change of THD with Switching Frequency at modulation index equals 0.5

The power loss and the efficiency for conventional and non-conventional 17- level are illustrated in Fig. (28) and Fig. (29) respectively. The two circuits have the same power loss and efficiency.

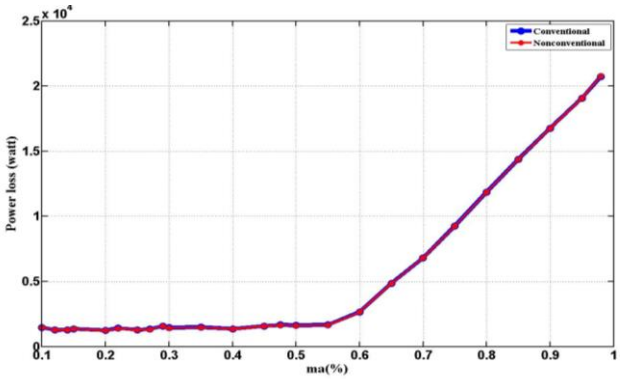


Figure (28): The Change Power Loss with m_a at constant switching frequency for Cascade 17-Level

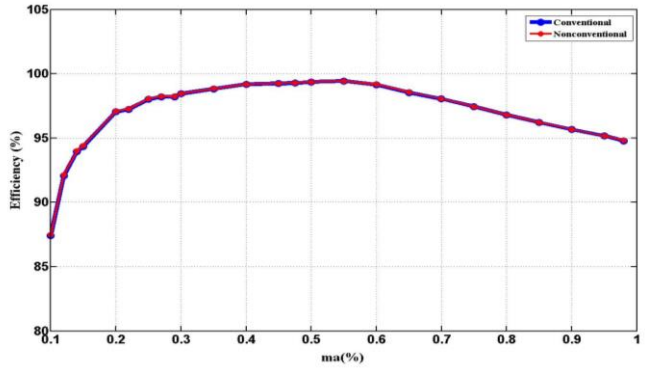


Figure (29): The Efficiency via m_a for Cascade 17-Level

In 17- level the conventional and non-conventional, the root mean square output voltage for different values of m_a is shown in Fig. (30).

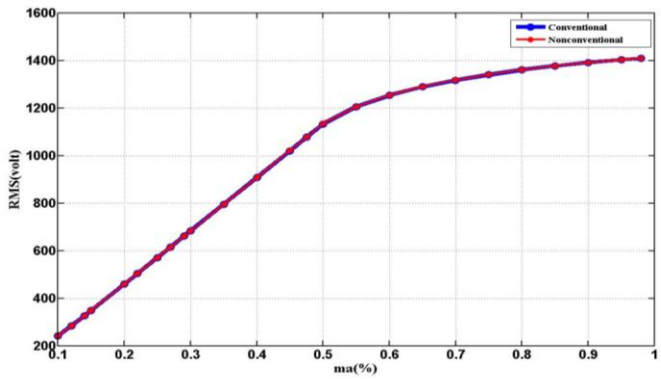


Figure (30): Change RMS Voltage with m_a at Constant Switching Frequency for Cascade 17-Level

When the circuits are operated using the HPWM technique, it is noticed that the same output voltage levels are produced with THD of 22.25 % which is higher than the PWM but the reason for using the HPWM is to avoid the overmodulation in the control circuit as shown in Fig. (31) and the results are shown in Fig. (32) and Fig. (33).

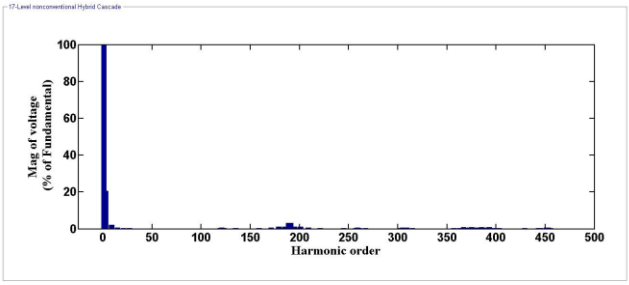


Figure (31): THD of output voltage waveform using HPWM

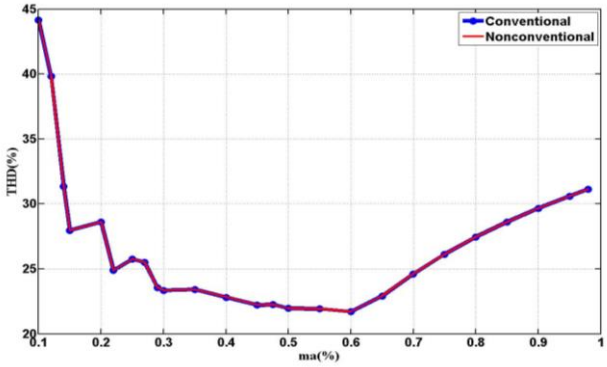


Figure (32): Change THD with m_a at Constant Switching Frequency using HPWM

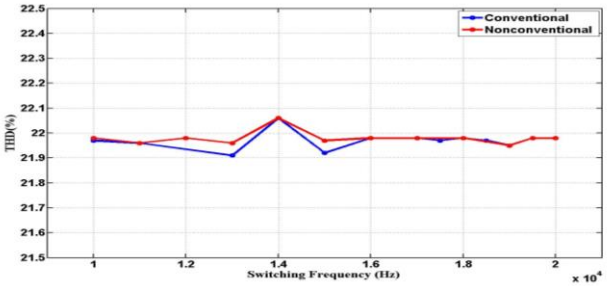


Figure (33): The Change of THD with Switching Frequency at a modulation index of 0.5 using HPWM

The efficiency and power loss of conventional and non-conventional for the same levels in HPWM control are convergent but the conventional circuit demands a large number of devices in the design also complex for control as shown in Fig. (34) and Fig. (35). It is clear that the loss increases for ma is high when all switches are turned ON.

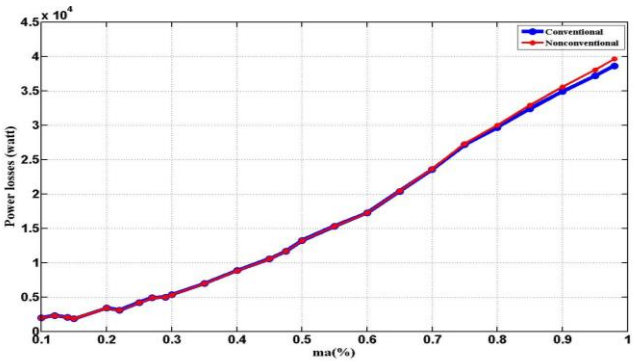


Figure (34): Change Power Loss with m_a at Constant Switching Frequency For HPWM Cascade by use HPWM

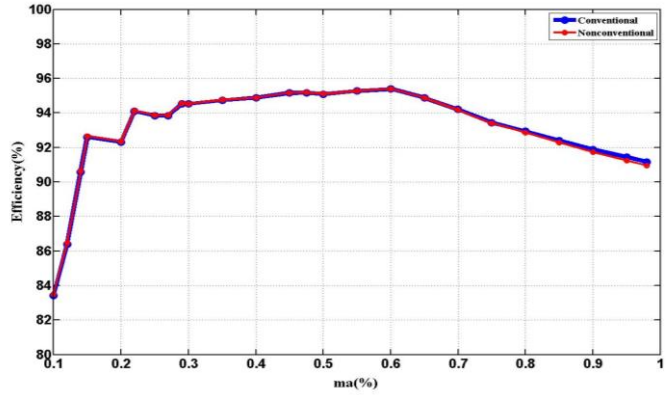


Figure (35): Change Efficiency with m_a at Constant Switching Frequency by use HPWM

When the same circuit operates with HPWM technique RMS voltage for 17- level illustrates in Fig. (37)

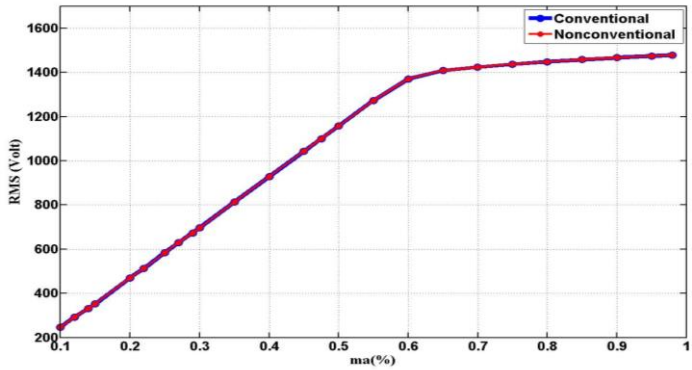


Figure (37): Change RMS Voltage with m_a at Constant Switching Frequency HPWM

Details in TABLE I clarify the comparison between conventional and non-conventional cascade of the two proposed topologies.

TABLE I
Comparison between conventional and Non-conventional cascade for 9 and 17 Level at $m_a = 0.55$

	Noncon. 9 Level	Conv. 9Level	Noncon 17Level	Con. 17Level
THD	12.1	12.14	6.89	6.89
Efficiency	98.47	98.4	99.43	99.43
Switching frequency	18000	18000	19000	19000
Power losses	1132	1172	1206	1651
RMS	716.5	706.6	1410	1409

VIII. CONCLUSION

This paper provides an analysis and comparison between conventional and non-conventional three phase nine level in the first topology and 17- level in the second topology. The main aim of these topologies is to reduce the number of devices. In the first topology, nine level is produced using eleven switches per phase, while the conventional one needs four H bridge (16 switches per phase) to produce the same number of level. The same is in the second topology of 17- level where the conventional needs eight H bridge (32 switches per phase) while the non-conventional needs 20 switches per phase. To verify the performance of each topology, the simulation results under resistive load can be used. It is clear from the results that non-conventional is coverage with conventional such as efficiency, THD, and power losses but the number of switches are less. Moreover, other advantages such as simple control, low cost, system size reduction, and switching loss can also extend to each type at a high level.

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